Figure 1
Prior Art Processor

(100)

Prefetch And Dispatch Unit 122

Instruction Cache And Buffer 124

Floating Point Register File 136

Integer Register File 138

Floating Point Execution Unit 128

Integer Execution Unit 126

Memory Management Unit 110

Load/Store Unit 112

External Cache Unit 114

Memory Interface Unit 118

External Cache 116

System Interconnect 120

RF-2   202

31   0

Bypass Circuit   206

Floating Point Execution Unit   214

• • •

Floating Point Execution Unit   212

RF-1   200

31   0

Bypass Circuit   204

Integer Execution Unit   210

• • •

Integer Execution Unit   208
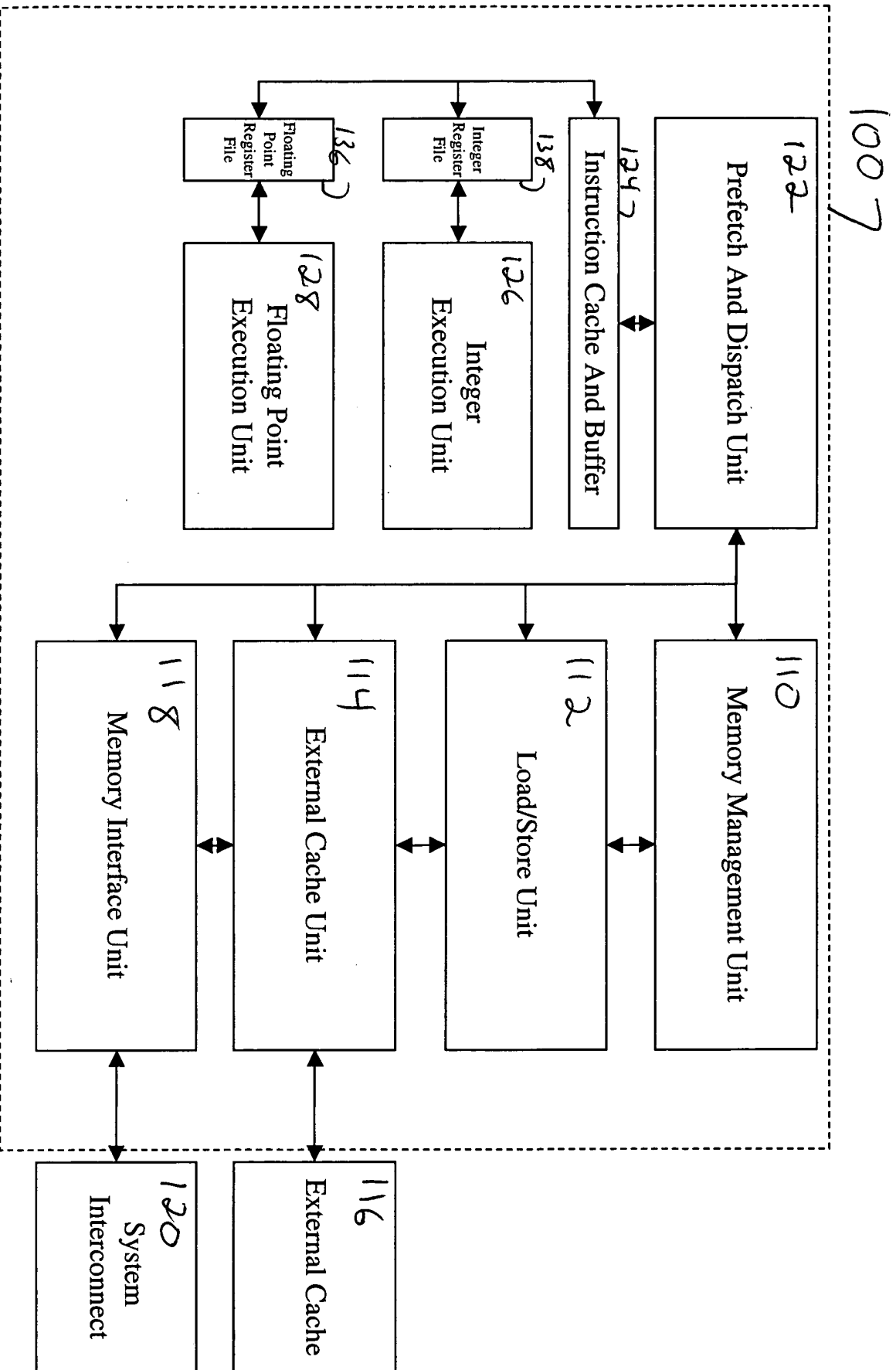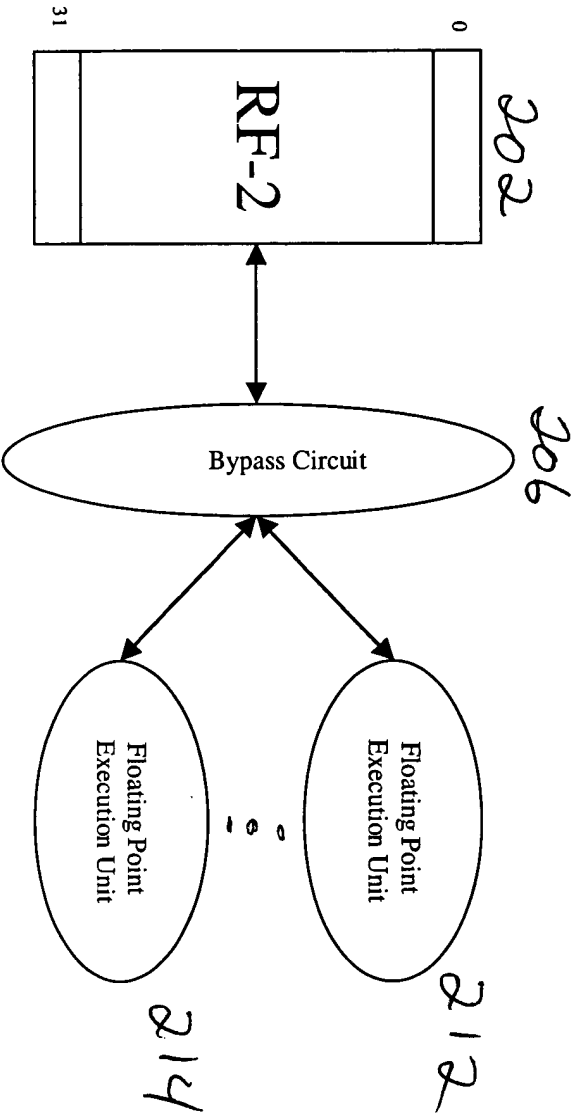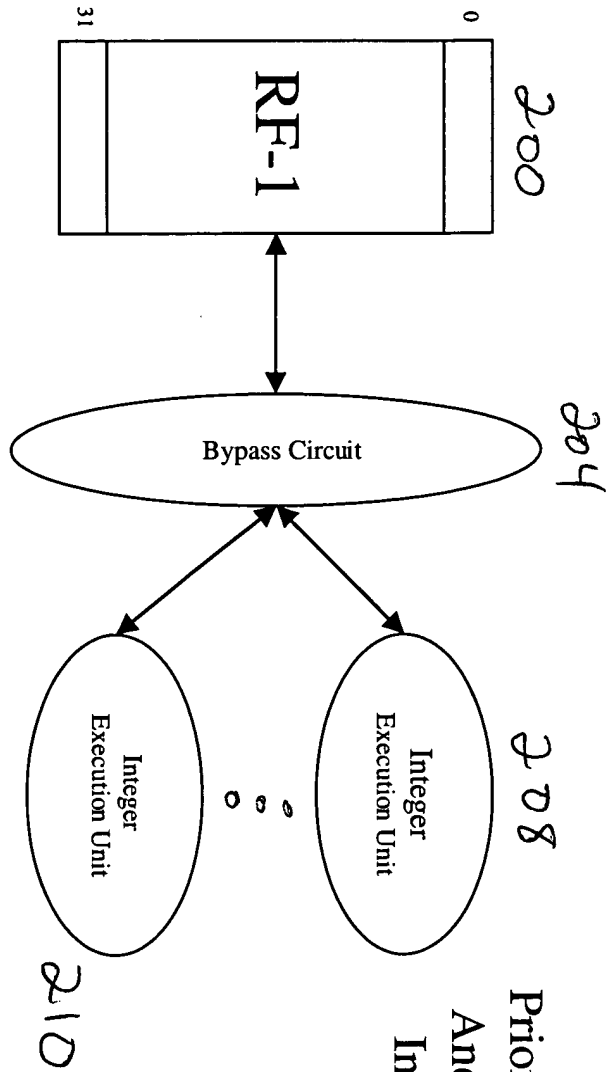
Figure 2
Prior Art Execution Units
And Register Files With
Increased Parallelism
Using Multiple
Execution Units

Figure 3
Execution Units And Backing
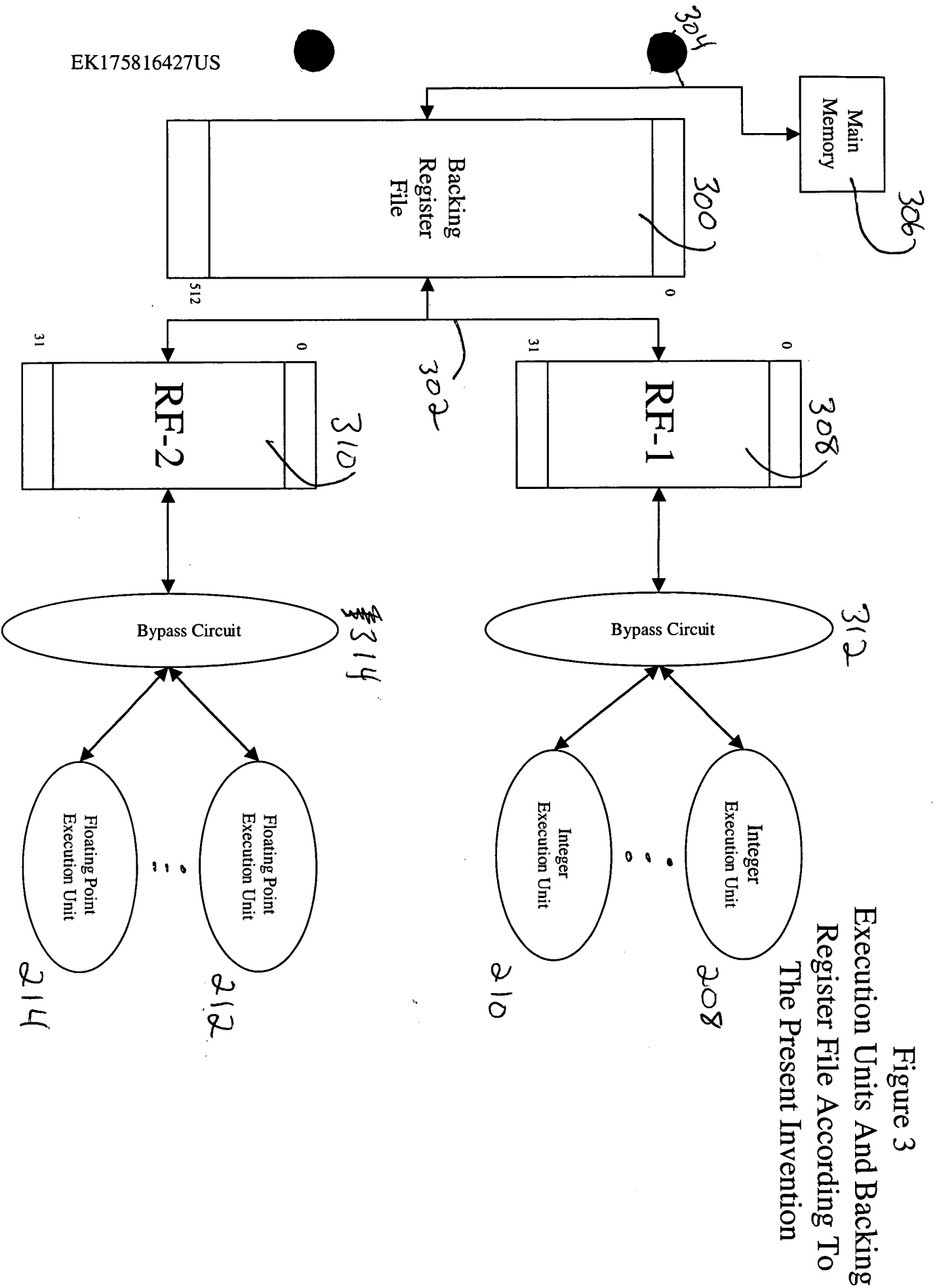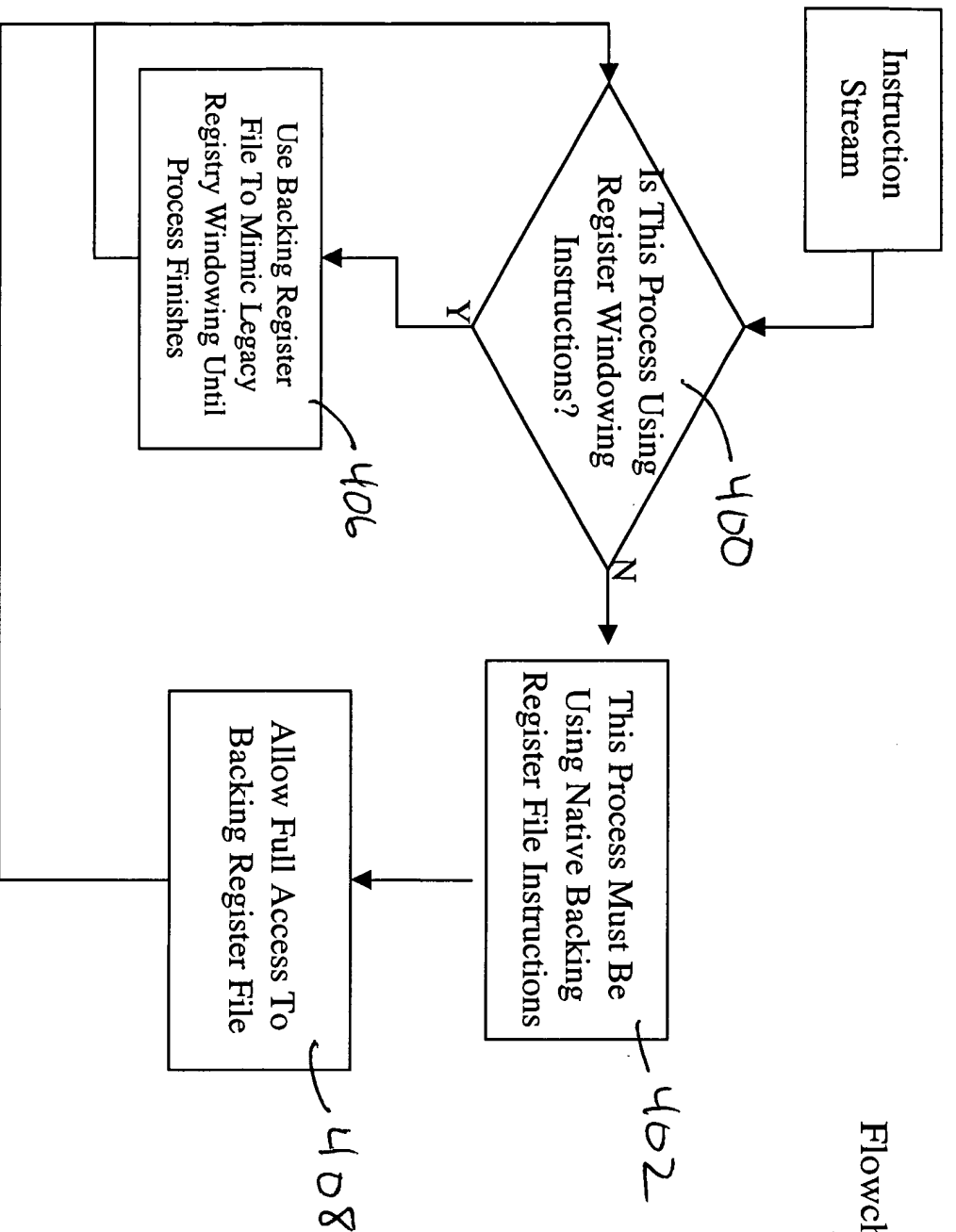Register File According To
The Present Invention

Instruction
Stream

Is This Process Using
Register Windowing
Instructions? 400

Y

Use Backing Register
File To Mimic Legacy
Registry Windowing Until
Process Finishes 406

N

This Process Must Be
Using Native Backing
Register File Instructions 402

Allow Full Access To
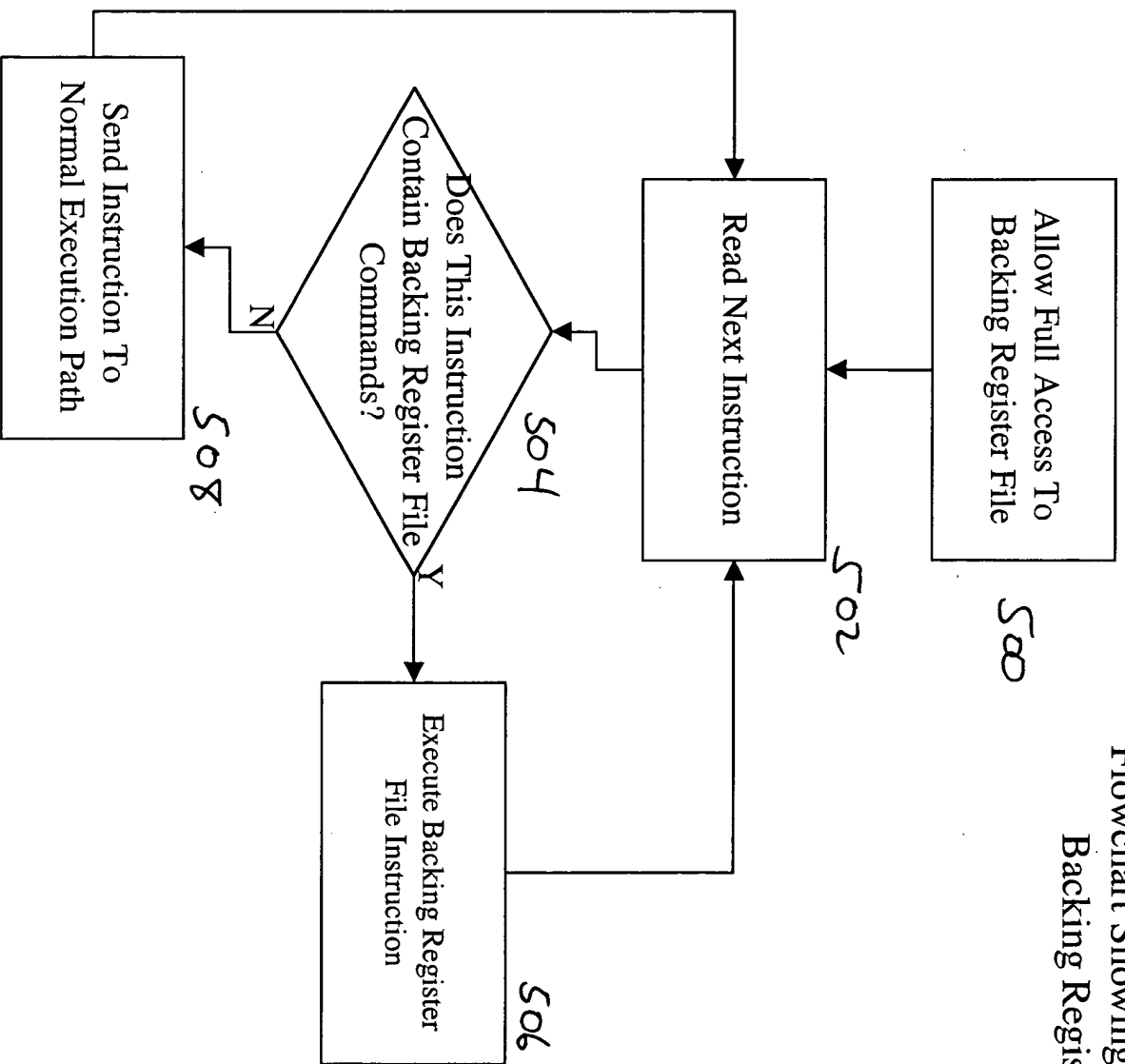Backing Register File 408

Figure 4
Flowchart Example Of Initializing
The Present Invention

Figure 5
Flowchart Showing Use Of The
Backing Register File

Figure 6a
Data Organization: Singly Linked List

Backing Register File Symbol

Send To Register File 1

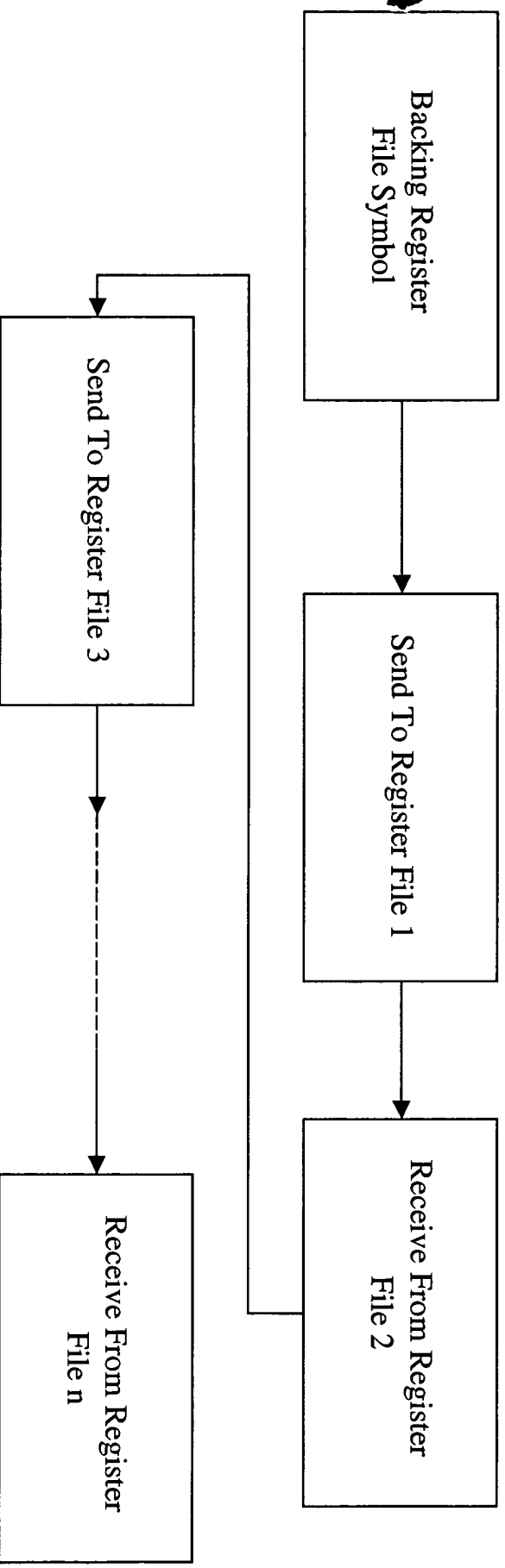Receive From Register File 2

Send To Register File 3

Receive From Register File n

Figure 6b
Data Organization: Byte Stream

| Backing Register File Symbol | Send To Register File 1 | Receive From Register File 2 | Send To Register File File 3 | Receive From Register File n |